ARMY RESEARCH LABORATORY

A Hybrid Multi-gate Model of a Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) Device Incorporating GaN-substrate Thermal Boundary Resistance

by Horacio C. Nochetto, Nicholas R. Jankowski, Brian Morgan, and Avram Bar-Cohen

ARL-TR-6228 **October 2012**

NOTICES

Disclaimers

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

Army Research Laboratory
Adelphi, MD 20783-1197

ARL-TR-6228 **October 2012**

A Hybrid Multi-gate Model of a Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) Device Incorporating GaN-substrate Thermal Boundary Resistance

Horacio C. Nochetto, Nicholas R. Jankowski, and Brian Morgan
Sensors and Electron Devices Directorate, ARL

and

Avram Bar-Cohen
Microsystems Technology Office, DARPA

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
October 2012	Final	

4. TITLE AND SUBTITLE
A Hybrid Multi-gate Model of a GaN High Electron Mobility Transistor (HEMT) Device Incorporating GaN-substrate Thermal Boundary Resistance

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Horacio C. Nochetto, Nicholas R. Jankowski, Brian Morgan, and Avram Bar-Cohen

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
ATTN: RDRL-SED-E
2800 Powder Mill Road
Adelphi, MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TR-6228

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
This report describes a pseudo-analytical thermal model of gallium nitride (GaN) high electron mobility transistors (HEMTs), which combines analytical heat spreading models with spreading width boundary conditions derived from two-dimensional finite element thermal simulations. We successfully produced an accurate GaN HEMT hybrid model capable of evaluating the impact of thermally important device parameters on junction and individual layer temperatures. A parameter space investigation, covering GaN-substrate thermal boundary resistance (TBR), gate pitch, substrate thickness, substrate thermal conductivity, and GaN thickness validated the hybrid model against full finite element numerical analysis and provided insight into device thermal behavior. This modeling showed "near junction" thermal resistance contributions from the GaN and interface TBR stay relatively constant with gate number and pitch down to 5 μm. Alternatively, the thermal profiles in the substrate layers and below show strong interaction between gates; the magnitude of those components scale directly with gate number and increase significantly with decreasing gate pitch. Also finite substrate and GaN thicknesses produce a minimum temperature rise dependent on downstream thermal resistance. Finally, increasing substrate thermal conductivity, by replacing a silicon carbide (SiC) substrate with higher thermal conductivity diamond, appears to only be advantageous if the TBR does not increase substantially beyond the SiC range.

15. SUBJECT TERMS
Gallium Nitride, HEMT, heat transfer, thermal boundary resistance, thermal model, finite element analysis

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Nicholas R. Jankowski
Unclassified	Unclassified	Unclassified	UU	42	19b. TELEPHONE NUMBER (*Include area code*) (301) 394-2337

Contents

List of Figures

List of Tables

INTENTIONALLY LEFT BLANK.

1. Introduction

The Department of Defense (DoD) is actively developing monolithic microwave integrated circuit (MMIC) technology to enable radio frequency (RF) systems with reduced component count and increased power density (*1*). Recently, quality improvements in gallium nitride (GaN) electronic materials and the development of the high electron mobility transistor (HEMT) device structure have allowed order-of-magnitude increases in both total power and power density over competing technologies (*2*). However, the operating efficiency of these devices is highly dependent on their operating frequency and temperature. Consequently, even high efficiency power amplifiers (PAs) require significant cooling to maintain high electrical performance and reliability (*3, 4*).

PA cooling is further complicated by the unique structure of GaN devices, which are fabricated on multi-material substrates optimized for electrical performance and not necessarily heat transfer. Moreover, the HEMT structure creates highly localized hot zones in the active area of the device. This results in a challenging thermal situation where heat spreading and interface resistances internal to the device can dominate the thermal profile, even when using high performance packaging and cooling structures.

There have been several past efforts at thermally modeling the GaN HEMT device. In the series of reports by Calame et al., the thermal performance of a GaN-HEMT package was numerically evaluated in a number of material and package configurations to examine the interaction of device- and package-level thermal effects (*5–7*). Darwish et al. have provided an analytical thermal resistance expression based on the solution of Laplace's equations in prolate steroidal coordinates and elliptical cylinder coordinates (*8, 9*). Douglas et al. studied the effects of several HEMT design parameters, including substrate thermal conductivity, gate number, and die size (*10*). These groups provided insights into device thermal behavior, but none addressed the issue of the inter-layer thermal boundary resistance (TBR) present in the GaN HEMT material stack between the GaN and substrate layers.

The University of Bristol recently reported that this TBR in commercial devices on silicon carbide (SiC) substrates can reach levels greater than 60 m^2K/GW, which can increase the device's maximum temperature by up to 40%–50% (*11–13*). In fact, previous work by the authors numerically modeled several single-gate GaN HEMT devices and demonstrated significant TBR influences on junction temperature trends (*14*). Yet, evaluating a large parameter space with this numerical approach to fully understand device design tradeoffs would require significant computational resources. It is thus advantageous to have accurate analytical models to initially guide designers towards their goals. Thermal spreading resistance models like those developed by Yovanovich, Muzychka, and Culman (hereafter referred to as YMC models) that solve heat diffusion using separation of variables while accounting for geometric, heating, and

convection cooling boundary conditions (*15, 16*) can provide accurate temperature distributions within the layers if the TBR is ignored. However, as our previous analysis showed, the TBR must be integrated into these solutions to provide an accurate parametric tool for designers (*14*).

Our work accomplishes this goal through a hybrid model that combines numerically determined spreading widths with the YMC spreading resistance models. These spreading widths are fitted to a two-dimensional (2-D) equation so that others may use the hybrid model as an initial design tool without further need of numerical models. Section 2 briefly reviews the GaN/HEMT architecture, common temperature remediation techniques, and recent experimentally determined TBR ranges for GaN on SiC devices. Following this background, the YMC spreading model's ability to predict HEMT temperature rise is briefly examined, focusing on the inability of the model and constant heat spreading assumptions to properly incorporate the effect of the TBR. We then use the YMC model as a major stepping stone in the description of a hybrid HEMT thermal model. Finally, the hybrid model is validated against 2-D finite element simulations of the device for parameters of TBR, gate to gate pitch, substrate thickness, substrate thermal conductivity, and GaN thickness.

2. Background

HEMT devices can be integrated into MMIC dies along with input and output circuits as shown by the example in figure 1.

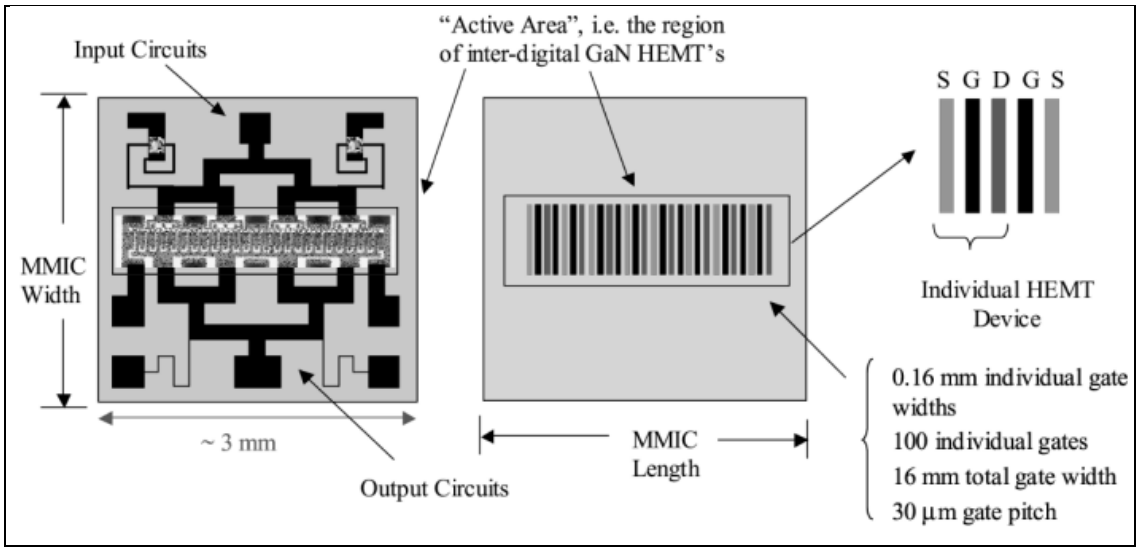


Figure 1. HEMT device on MMIC die (*5*).

Within the active area, there are many individual transistor unit cells comprised of a source (S), drain (D), and gate (G) electrodes atop a multilayered semiconductor structure. The structure's specific composition can vary widely, two examples of which are shown in figure 2. In addition

to the layers shown in the figure, the top of the devices are typically coated with silicon nitride (SiN) for surface charge passivation (not shown) (*18*).

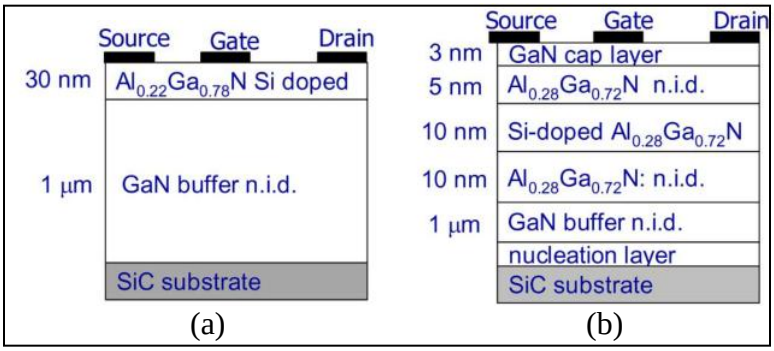


Figure 2. Example GaN HEMT structures, including (a) simple and (b) complex layer configurations (*17*).

Localized heat zones have been previously modeled and experimentally verified to occur adjacent to the gate in the active aluminum gallium nitride (Al_xGaN_{1-x}) layer (*18*). This layer can vary in composition, and consequently also in its effective thermal conductivity. Liu and Baladin (*19*) benchmarked several Al_xGaN_{1-x} compositions through a wide range of temperatures and showed a thermal conductivity range of 25–125 W/mK at 300 K and 25–110 W/mK at 400 K. However, to provide a simple hybrid model for initial parameterization, our work simplifies the active layers into a single homogenous Al_xGaN_{1-x} layer and employs temperature-independent material properties.

The active Al_xGaN_{1-x} and GaN device layers are grown on a silicon (Si) or SiC substrate due to the unavailability of single crystal GaN. However, the crystal mismatch between the GaN and substrate materials requires intermediary aluminum nitride (AlN) buffer layers to reduce the number of lattice defects that would propagate up to the critical GaN layers. The remediation of these lattice defects increases electrical performance, but the buffer layers' poor thermal conductivity hinders heat transfer. Thus, the low thermal conductivity of the buffer along with the lattice mismatch between the GaN and the substrate create a substantial TBR (*11, 20*). This TBR exacerbates the thermal impact of the localized hot zones causing elevated near junction temperatures, a reduction in the maximum power density, and accelerated device failure (*21, 22*).

As such, the remediation of the junction temperature has become a major concern. Several groups have studied the thermal impact of gate to gate pitch, such as Yamanaka et al., who demonstrated that the doubling of the gate to gate pitch from 15 to 30 μm can provide 56 °C lower temperatures (at equal power) or a 1.4 times increase in total power density (at equal temperature) (*23, 24*). Others studied the impact of high thermal conductivity substrates such as SiC (*10*) and chemical vapor deposition (CVD) diamond (*4, 25, 26*), with the latter containing a substrate removal and attachment process, which contains a proprietary GaN-substrate attachment layer. More information regarding these remediation techniques, as well as layer thinning, can be found in references 4, 8, and 27–30.

2.1 GaN-substrate Thermal Boundary Resistance

The calculation and measurement of TBR in GaN HEMT devices is an ongoing process. The TBR of an ideal GaN/SiC interface was calculated using the diffuse mismatch model (DMM) to be around 1 m²K/GW (*31*). This, however, only accounts for the diffuse mismatch between the GaN and SiC layers and does not account for the low thermal conductivity transition layers that contribute to the TBR. Consequently, this model under predicts recent experimental measurements by one to two orders of magnitude (*11*).

Manoi et al. thermally benchmarked state-of-the-art HEMT TBRs from American, Japanese, and European manufactures that all used metal-organic chemical vapor deposition (MOCVD), but different buffer layer growth parameters (*11*). Since the buffer layer is optimized for electrical and not thermal performance, a wide TBR range between 10 m²K/GW and almost 70 m²K/GW was shown to exist because of microstructure defects (*11, 12*). Sommet et al. inversely determined for a single sample using finite element analysis (FEA) that the GaN/SiC interface defects cause a TBR of 22 m²K/GW, which falls within the previously stated range (*32*). The defects cause increased phonon scattering, which, in turn, reduces the effective conductivity of the buffer layers, increase the HEMT interlayer TBR, and consequently increases the maximum temperature rise by 10%–40% when compared to a device with no TBR (*11, 33, 34*). Thus, the TBR is a vital component of an accurate GaN HEMT thermal model.

2.2 Examination of Existing Predictive Model

With such elevated temperatures directly attributed to the TBR, any analytical model expected to be used as an initial parametric tool should accurately capture TBR-related effects. One possible candidate, the single and double Yovanovich, Muzychka, and Culman models (single and double YMC models), detailed in references 15 and 16, use an infinite series solution to provide the maximum temperature of a layered structures similar to the GaN HEMT geometry of interest. The model incorporates a convective heat removal boundary condition, which allows it to capture heat spreading as a function of downstream thermal resistance, producing increased accuracy when compared to fixed heat flux or temperature boundary condition models.

Using the GaN thickness trend as a benchmark, the YMC two-layer model was compared against the 2-D finite element results for a GaN HEMT with no TBR present. The heat source's small dimensions relative to the total gate width justifies the use of a 2-D model near the heat source. For the purpose of this initial study, we extend the use of the 2-D model to the entire device despite the discrepancy that may develop in the substrate due to three-dimensional spreading effects farther from the gate. Figure 3 shows that for the baseline parameters and no TBR, the YMC two-layer model can accurately capture the expected trends.

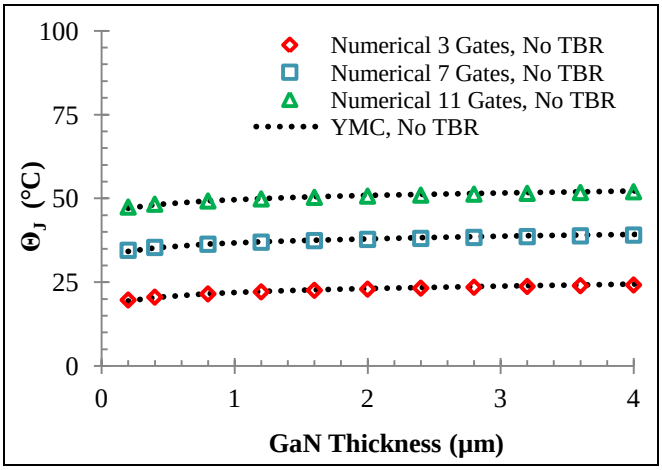


Figure 3. Junction temperature as a function of GaN thickness and gate number for numerical and YMC models (no TBR and table 1 parameters).

Unfortunately, GaN HEMTS contain a TBR ranging from 10–70 m²K/GW (*11*, *12*), which cannot be directly incorporated within the YMC two-layer model. Attempting to directly add the TBR temperature rise as a contact resistance to the YMC two-layer model results in trends similar to figure 4. The results in the figure assume a constant 55° spreading angle in the GaN layer, which is a commonly used but rather inaccurate method of determining the actual width of the heat path across the boundary. For the 10 m²K/GW TBR case shown, junction temperatures below 1 µm should remain relatively constant as the GaN thickness decreases. However, the constant 55° spreading angle modified YMC model over-predicts the numerical trends for most GaN thicknesses of interest. In fact, the shape of the YMC curves suggest that the fixed spreading approximation uncoupled from the actual spreading solution over-constrains the model and imposes excessive temperature rise.

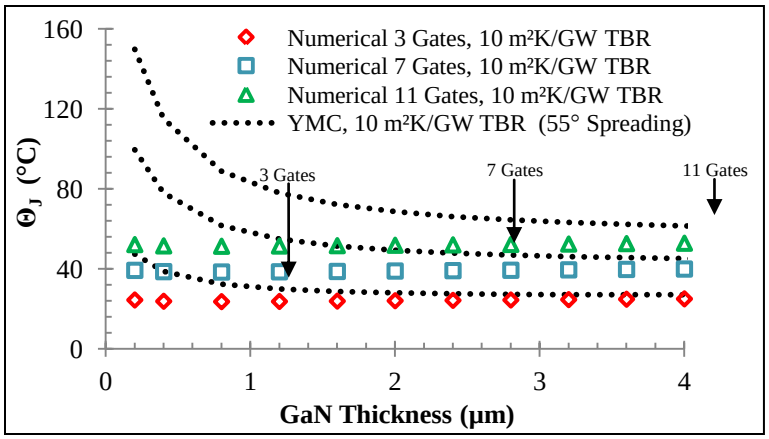


Figure 4. Junction temperature as a function of GaN thickness and gate number for numerical and YMC models (10 m²K/GW TBR and table 1 parameters).

Clearly, the constant spreading angle assumption imposed on an analytical model is not sufficient to produce accurate results. In addition, even if approximate spreading angles were

extracted from numerical simulations like that in reference 14, and a spreading angle profile similar to that shown in figure 5 was produced, the GaN and substrate components would still not be coupled with the TBR component. Individual layer spreading would not be affected, and ultimately inaccurate and misleading results would be produced by such a model. Thus, the goal of our study is to develop an accurate thermal model for GaN HEMTS that couples heat spreading and TBR effects and can be used as a design tool for improving thermal performance.

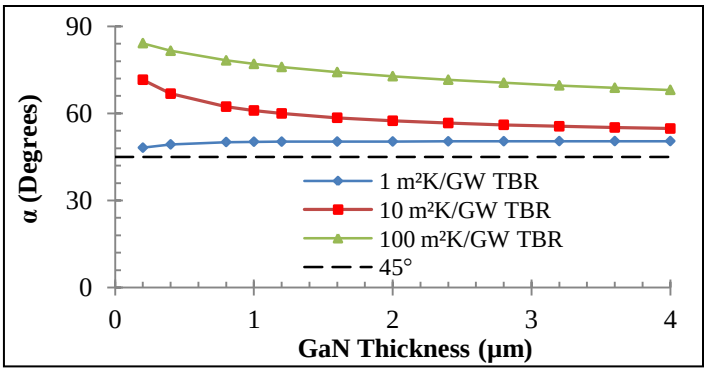


Figure 5. Spreading angle as a function of GaN thickness (table 1 parameters).

3. Hybrid Model

As in the previous numerical study, our GaN HEMT model accounts for the highly localized heat originating in the Al_xGaN_{1-x} and spreading through the device layers, including crossing the GaN-substrate TBR (*14*). This model takes a hybrid approach by combining 2-D analytical YMC heat spreading models with extracted numerical models of the parameter-dependent heat spreading behavior.

As shown by figure 6, the hybrid model splits the geometry into two single-layer domains at the GaN-substrate interface. This enables both the insertion of a discrete TBR and the incorporation of that resistance into single-layer heat spreading models. However, the single-layer YMC models used to calculate the thermal resistances and temperature distributions require uniform heating and cooling heat transfer coefficients as boundary conditions. Because the actual thermal profiles at this interface are expected to be non-uniform (*35*), the hybrid model iteratively develops uniform boundary conditions that approximate the numerical results. For the substrate, the external convective boundary condition (h_{CP}) is applied to its lower surface while heat is uniformly applied across a line that is as wide as the numerically determined spreading width (L^*). For the GaN layer, heat is uniformly applied at the top to account for the device heat source. At the bottom of the GaN, a uniform convective boundary condition is applied whose coefficient (h_{GaN}) incorporates the effect of the TBR and other downstream resistances.

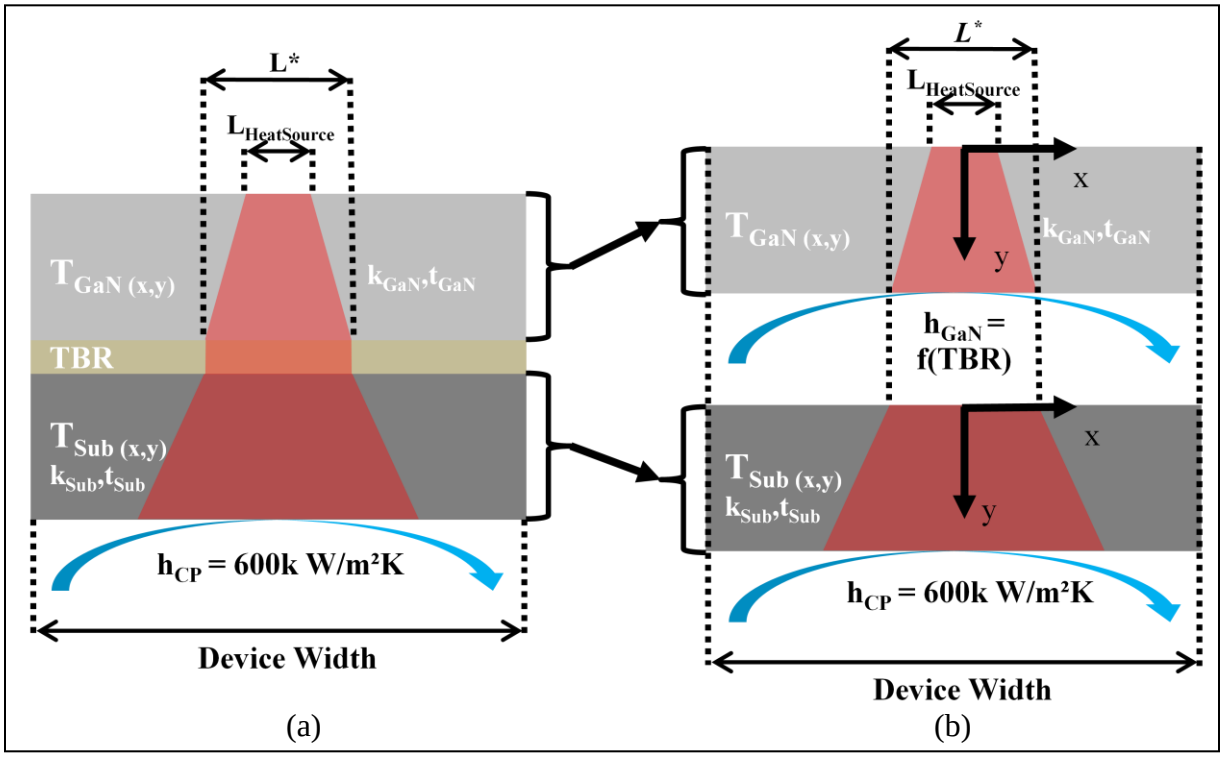


Figure 6. (a) Two layer model with TBR and (b) hybrid model schematic showing separate layer domains with artificial coupling convection, h_{Gan}.

Application of the hybrid model can be more easily understood using the flow chart in figure 7. To begin, a numerical FEA model (similar to reference 14) is used to determine the component of temperature rise due to the TBR. The spreading width (L^*) is then approximated as the width over which a uniform heat load of equal magnitude to the input heat creates the same peak temperature rise as that calculated numerically for the given TBR ($\Delta T_{Num,TBR}$). This is essentially a uniform, one-dimensional (1-D) thermal resistance calculation, as specified by

$$\Delta T_{Num,TBR} = q_s R_{TBR} = q'_s R'_{TBR} = q'_s \frac{TBR}{L^*} \quad (1)$$

where q'_s is the single heat source heat in W/mm, *TBR* is the thermal boundary resistance in m^2K/GW, and R_{TBR} is the TBR's corresponding thermal resistance in K/W. As shown in figure 8, this approximates the actual bell shaped heat flux profile at the GaN-substrate interface by a rectangular profile of length L^* and of height q'_s. This simplified heat distribution serves as the uniform heat input profile required for the lower layer of the model.

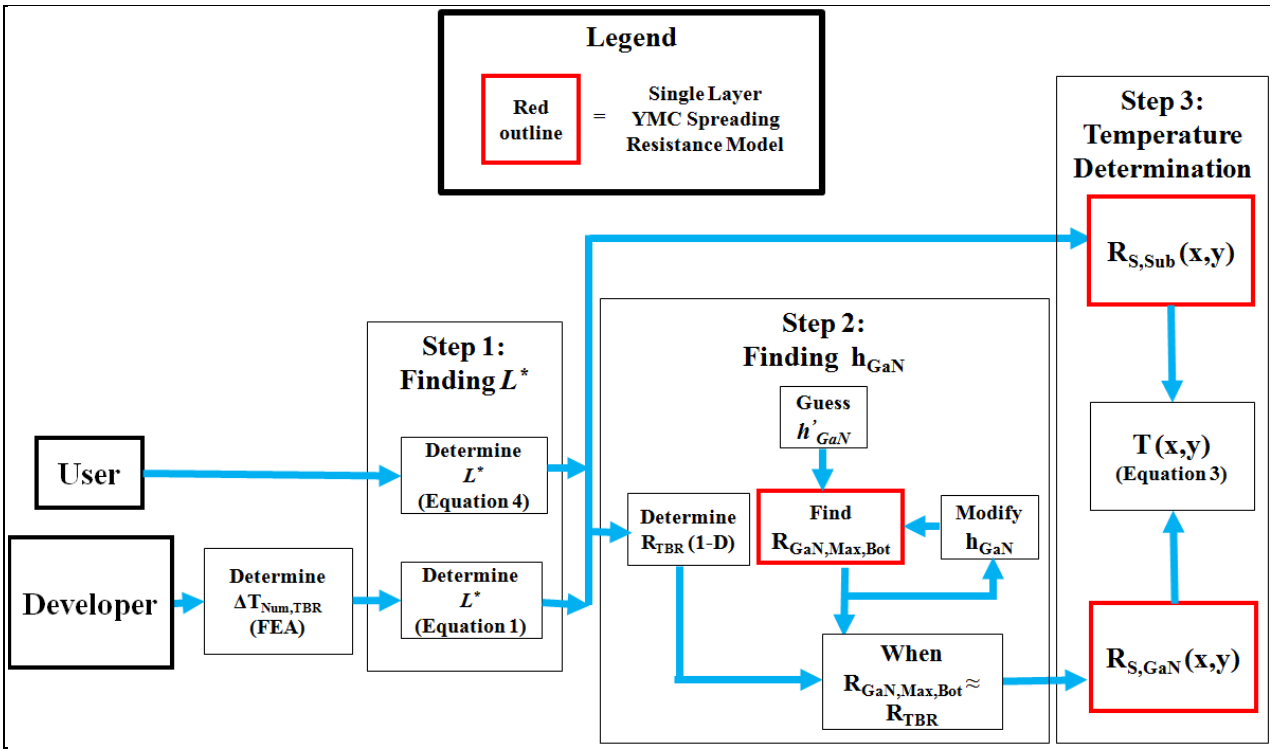


Figure 7. Hybrid model flow chart.

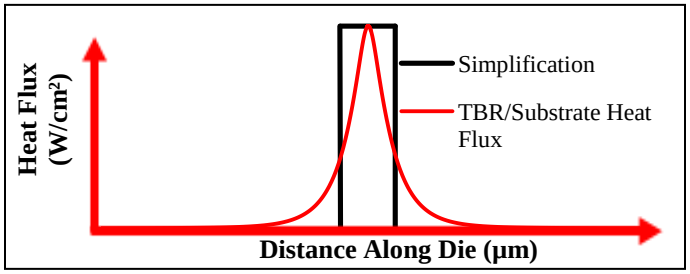


Figure 8. Comparison between actual lateral temperature profile due to TBR and L* simplification

In Step 2, h_{GaN} is iteratively determined for the upper layer model starting with an initial guess, h'_{GaN}, obtained from the one dimensional thermal resistance model shown in equation 2:

$$h'_{GaN} = \frac{1}{L^*\left(R_{TBR}' + R_{Sub.}' + R_{CP}'\right)} \quad (2)$$

where R_{Sub}' and R_{CP}' is the total thermal resistance in °C/(W/mm) of the substrate and cold plate respectively. An exact model would use a non-uniform convection coefficient profile at the interface, as shown in figure 9a for a representative case, and the value of h_{GaN} in equation 2 closely approximates the average value of that profile. Because the average value fails to account for heat spreading, it results in a much higher total thermal resistance as shown in figure 9b. Thus, the hybrid model iteratively determines the single value heat transfer coefficient that

matches the peak thermal resistance at the bottom of the GaN layer ($R_{S,GaN}(0,0)$), as shown in figure 9b, but diverges from the numerical curve as the distance increases.

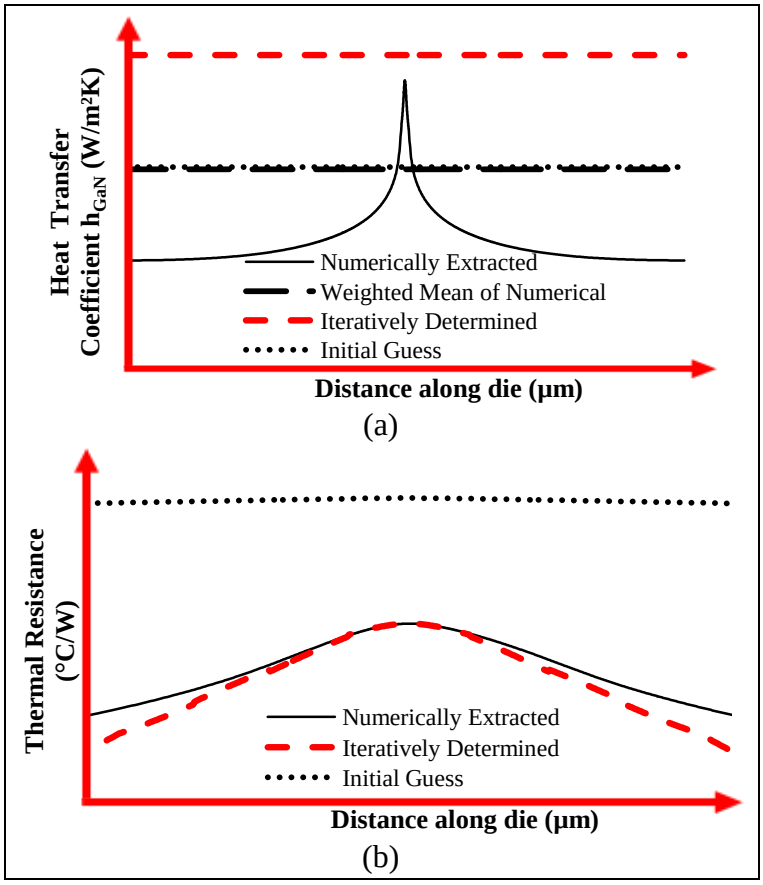


Figure 9. (a) Heat transfer coefficient applied to the bottom of the GaN layer and (b) thermal resistance on the bottom of the GaN layer.

In Step 3, the GaN and substrate layer's spreading resistances ($R_{S,GaN}$ and $R_{S,Sub}$) are determined using the YMC spreading resistance model and the necessary input and boundary conditions identified in Steps 1 and 2 of the flow chart in figure 7. These resistances are subsequently summed with their corresponding 1-D counterparts ($R_{1\text{-}D}$) following conventions discussed in reference 16 though the relationship in equation 3:

$$T_{Sub}(x,y) = Q_s\left(R_{S,Sub}(x,y) + R_{1D,Sub}(y) + R_{CP}\right)$$
$$T_{GaN}(x,y) = Q_s\left(R_{S,GaN}(x,y) + R_{1D,GaN}(y)\right) + T_{Sub}(x,0) \quad (3)$$

The TBR (T_{TBR}) and cold plate (T_{CP}) temperature distributions as well as the maximum temperature for a single gate (T_{SGJ}) are subsequently determined though the relationships in equation 4:

$$T_{TBR}(x) = T_{GaN}(x, t_{GaN})$$
$$T_{CP}(x) = T_{Sub}(x, t_{Sub}) \quad (4)$$
$$T_{SGJ} = T_{GaN}(0,0)$$

These single-gate temperature distributions are then superimposed (heat per gate is constant) for multi-gate device results.

4. Case Study

Our work models multi-gate GaN/HEMT devices, with 0.5-µm-wide heat sources within the Al_xGaN_{1-x} layer on the drain side of the gate. This location was previously demonstrated through micro-Raman/infrared thermography by Saura et al. (*18*) and numerically used in reference 14. For this study the 2-D model of the transistor domain in figure 10 uses device geometries from reference 18. The materials listed in table 1 are assumed to be temperature independent in both the hybrid and numerical models.

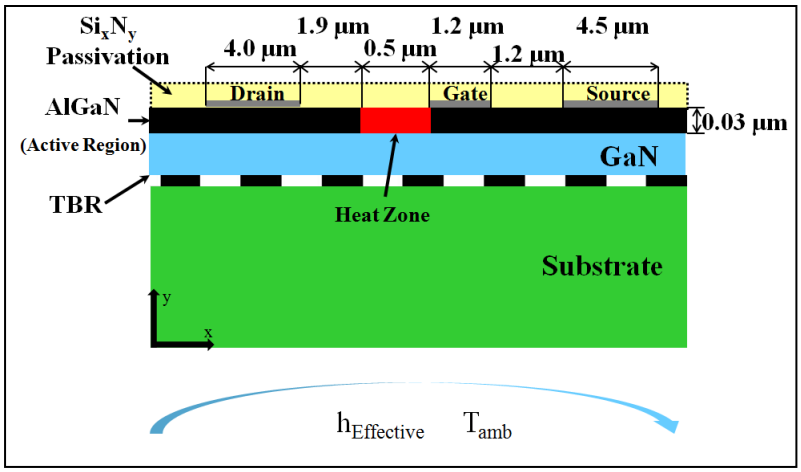


Figure 10. The 2-D single-gate GaN HEMT, with geometries adopted from reference 18.

Table 1. HEMT layer thicknesses and thermal conductivities at 300 K (*14*).

SiC Substrate	**300 µm**	**400 W/mK**
GaN	1.0 µm	130 W/mK
Al_xGaN_{1-x}	0.03 µm	30 W/mK
Gold Metal contacts	0.15 µm	315 W/mK
Si_xN_y Passivation	0.1 µm	15 W/mK
Pitch	13.3 µm	
Gate Number	11	
TBR	10 m²K/GW	

Temperature-independent material properties and ignoring edge effects facilitate the use of equation 5 to perform superposition of *n* gates at each component interface. Each single-gate temperature distribution ($T_s(x)$), whether it be the GaN, TBR, substrate, or the cold plate, is translated $(n–1)/2$ times to the left and right by a pitch (P) and subsequently summed to provide a multi-gate superimposed temperature distribution ($T_{MG}(x)$). An example is shown in figure 11.

$$T_{MG}(x) = \sum_{i=2,4,6\ldots}^{n} T_S\left(x + \frac{i}{2}P\right) + \sum_{i=1,3,5\ldots}^{n} T_S\left(x - \frac{i-1}{2}P\right) \quad (5)$$

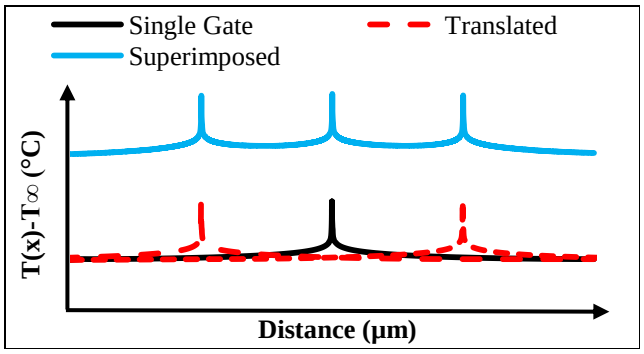


Figure 11. Superposition principle.

High-performance device power levels in recent years are on the order of 1–10 W/mm, with laboratory demonstrations in the range of 40 W/mm (*36*, *37*). The uniform material property assumption retains model linearity, allowing us to normalize all temperatures to an applied heat load of 1 W/mm (gate width) in the present study as shown by 2-D numerical temperature contour model in figure 10.

An effective heat transfer coefficient applied to the bottom of the substrate accounts for any downstream resistances between the substrate and cooling liquid including solder, spreaders, thermal interface materials (TIM), and a cold plate. A 600 kW/m²K effective heat transfer coefficient was used throughout this study to approximate a highly efficient cooling solution similar to the one suggested by Garven and Calame in reference 35.

The parameter space for this study is summarized in table 2. The single-gate numerical model was built with the commercial FEA software, ANSYS 13.0.

Table 2. Model parameter space.

Parameter	Range
Gate Number	3–11
Gate to Gate Pitch (µm)	3–50
TBR (m²K/GW)	0–100
GaN/SiC TBR (m²K/GW)	10–100
Isotropic Substrate Thermal Conductivity (W/mK)	100–2000
Substrate Thickness (µm)	25–500 µm
GaN thickness (µm)	0.2–4 µm

A high order 2-D thermal element, Plane77, is used to describe Fourier conduction, and 2-D contact and target elements, CONTA172 and TARGE169 are used to introduce the TBR. Meshes

showed convergence around 500,000 elements, with less than a 0.5 °C difference with double the element count. Figure 12 provides a single-gate GaN/HEMT temperature distribution produced by FEA.

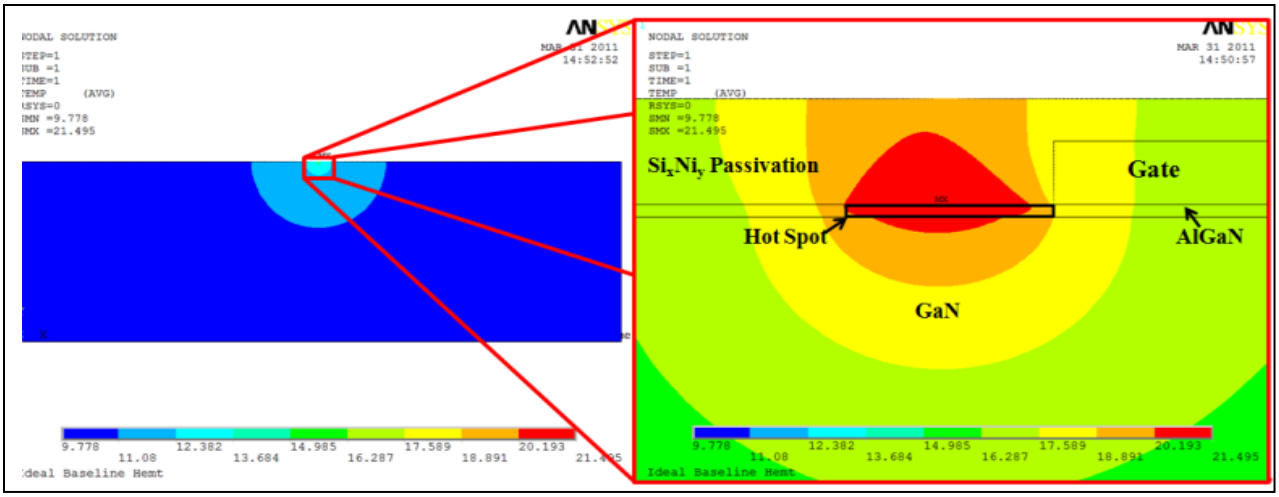


Figure 12. FEA extracted single-gate GaN HEMT temperature distribution (table 1 parameters and no TBR) (*14*).

4.1 Spreading width (L^*)

The spreading width parameter, L^*, is derived from the numerical model using equation 1 for the present geometry and the device parameters of TBR, substrate thickness, substrate thickness, and GaN thickness. These values are subsequently surface fitted into a multidimensional equation. Figure 13 provides a sample of the spreading width's dependence on TBR, primarily due to the significantly increased downward thermal resistance.

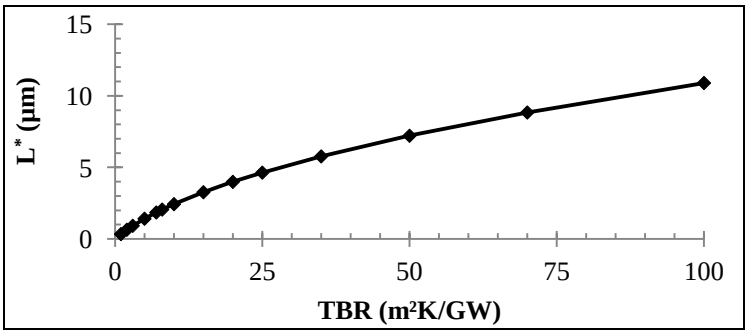
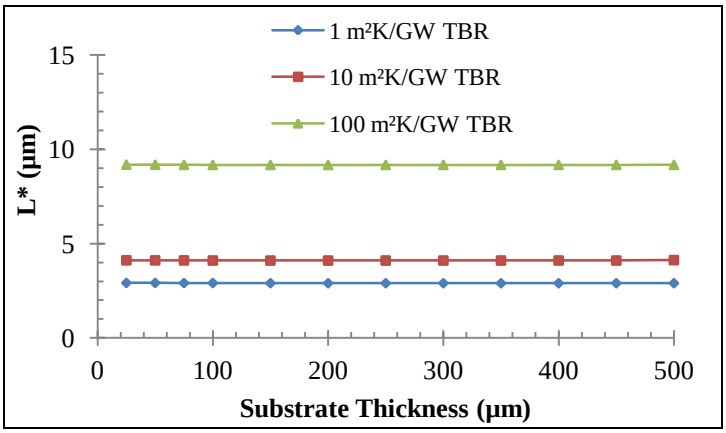
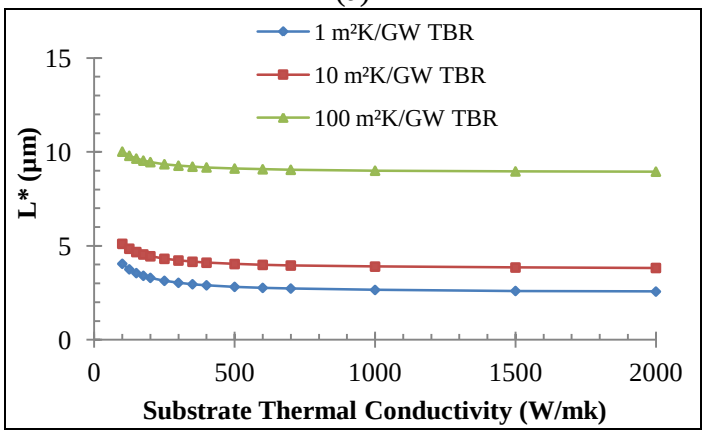


Figure 13. Spreading width L^*, as a function of TBR (single-gate table 1 parameters).

Figure 14 displays the spreading width as a function of TBR, substrate thickness and substrate thermal conductivity. The spreading width is relatively insensitive to substrate thickness and thermal conductivity for the present solution space. Only slight conductivity dependence is seen for substrate thermal conductivities less than 200 W/mK, and as such, will be neglected.



(a)



(b)

Figure 14. Spreading width, *L**, for multiple TBR values as a funciton of (a) substrate thickness, and (b) substrate thermal conductivity (single-gate table 1 parameters).

In addition to TBR, the other main contributor to spreading width variance is GaN thickness. As shown by figure 15, the spreading width increases quasi-linearly as the GaN thickness grows for the typical TBR range, with large TBR values (~100 m²K/GW) beginning to show a nonlinear behavior for small GaN layer thickness. Fortunately, the previously mentioned TBR measurements (*11*, *12*, *32*) have demonstrated typical GaN-on-SiC values between 10 and 70 m²K/GW. Given this, a linear approximation for the GaN thickness dependence will be used. If further accuracy is later needed at high values of TBR, a quadratic or other nonlinear approximation for this component can be used.

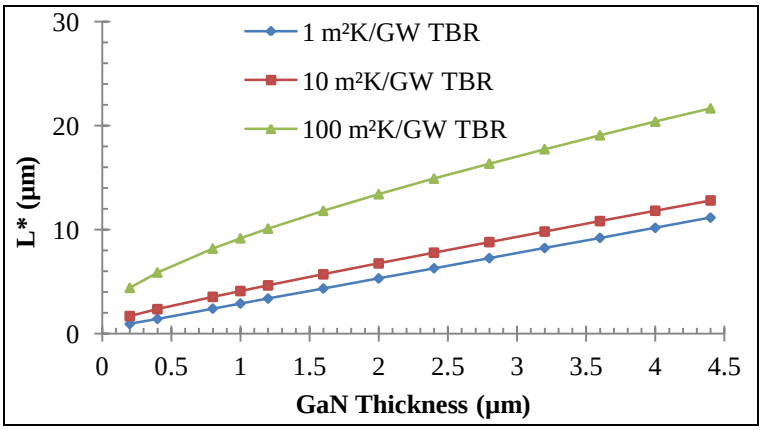


Figure 15. Spreading width, L^*, as a funciton of TBR and GaN thickness (single-gate Table 1 parameters).

Summarizing the above simplifications, the spreading width equation assumes linear dependence on GaN thickness and quadratic dependence on TBR. This facilitates the use of the surface fitting procedure by Nochetto (*38*) to provide the 2-D spreading width shown in equation 6, where g represents the GaN thickness in µm and TBR represents the thermal boundary resistance in m^2K/GW. For the parameter space given in table 2, the surface fit is shown graphically in figure 16 along with the corresponding error between the surface fit and the FEA derived values.

$$L^*(g,TBR) = c_1 + c_2 TBR + c_3 TBR^2 + c_4 g + c_5 g TBR + c_6 g TBR^2 \quad (6)$$

where

$$\begin{bmatrix} c_1 \\ c_2 \\ c_3 \\ c_4 \\ c_5 \\ c_6 \end{bmatrix} = \begin{bmatrix} 9.819 * 10^{-1} \\ 4.276 * 10^{-2} \\ -4.585 * 10^{-5} \\ 2.454 \\ 1.705 * 10^{-1} \\ -1.608 * 10^{-5} \end{bmatrix}$$

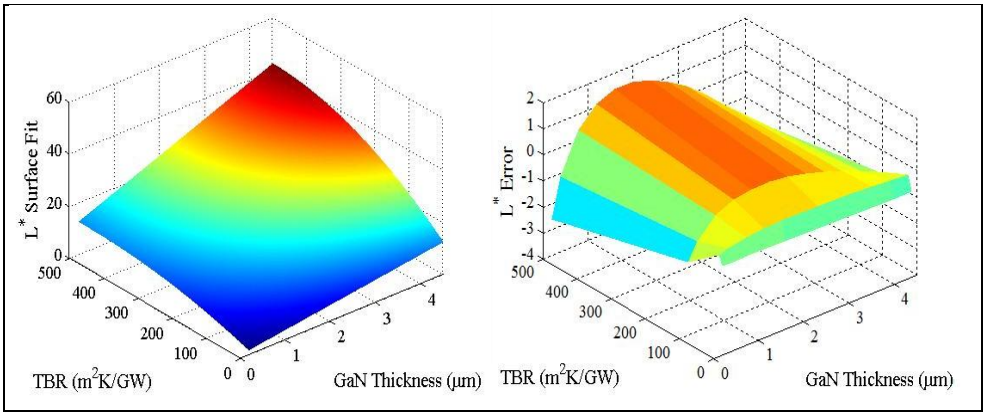


Figure 16. Surface fit spreading width, L^*, and the corresponding difference between the surface fit and the actual values.

4.2 Thermal Metrics

The hybrid model produced results, which were evaluated using the following metrics. Equation 7 defines Θ_J as the junction temperature rise over the coolant, or the difference between the centerline multi gate junction temperature on the upper surface ($T_{MG,GaN}(0)$) of the GaN and coolant temperatures (T_C).

$$\Theta_J = T_{MG,GaN}(0) - T_C \tag{7}$$

The cold plate temperature rise is defined in equation 8 as the difference between the maximum substrate bottom side temperatures and the coolant temperature (T_C).

$$\Theta_C = T_{CP}(0) - T_C \tag{8}$$

Each individual layer temperature rise is defined as the difference between the top and bottom maximum interface temperatures as shown by equation 9.

$$\begin{aligned} \Theta_{GaN} &= T_{GaN}(0,0) - T_{GaN}(0,t_{GaN}) \\ \Theta_{TBR} &= T_{TBR}(0) - T_{Sub}(0,0) \\ \Theta_{Sub} &= T_{Sub}(0,0) - T_{Sub}(0,t_{Sub}) \end{aligned} \tag{9}$$

The component discrepancy (Θ_{Dis}) between the numerical (Θ_{Num}) and hybrid models (Θ_{Hybrid}) is defined as their difference as shown by equation 10.

$$\Theta_{Dis} = \Theta_{Num} - \Theta_{Hybrid} \tag{10}$$

5. Results and Discussion

The previously described hybrid model is now compared to a 2-D numerical GaN HEMT model similar to those obtained in reference 14 for the parameters of TBR, gate-to-gate pitch, substrate thickness, substrate thermal conductivity, and GaN thickness. For all results presented, the hybrid model employs the spreading width equation 6.

There are several differences between the numerical and hybrid model that are expected to introduce some level of solution discrepancy. The numerical model contains metal contacts, an Al_xGaN_{1-x} layer, and a passivation layer above the GaN layer, none of which are included in the hybrid model. It does not appear that these differences significantly contribute to any discrepancy. Another major difference is that the numerical model applies uniform heat generation within the Al_xGaN_{1-x} layer (following references 14 and 18) and the hybrid model applies a uniform heat flux to the top of the GaN layer. This assumption is expected to be the primary contributor to any GaN layer discrepancy. Any TBR temperature rise discrepancy is expected to occur, because of the choice of a linear GaN thickness dependence in the

multidimensional spreading width equation (equation 6). Finally, the substrate temperature discrepancy arises due to the simplification of the top heat flux from a "bell-like" to a uniform shape as depicted in figure 8.

5.1 Effect of TBR

Figure 17 displays the junction temperature rise as a function of TBR for multiple gate numbers. Logically, an increase in TBR also increases the junction temperature. The portions of the structure that contribute to this increase are shown by the hybrid model layer temperature rise shown in figure 18a. At the prescribed geometry and boundary conditions, an increase of TBR mainly increases its respective temperature rise without much impact on the other components. Also, it is worth noting that the input power boundary condition fixed at 1 W/mm per gate results in increased total power for models with more gates, thus elevating the total temperature rise.

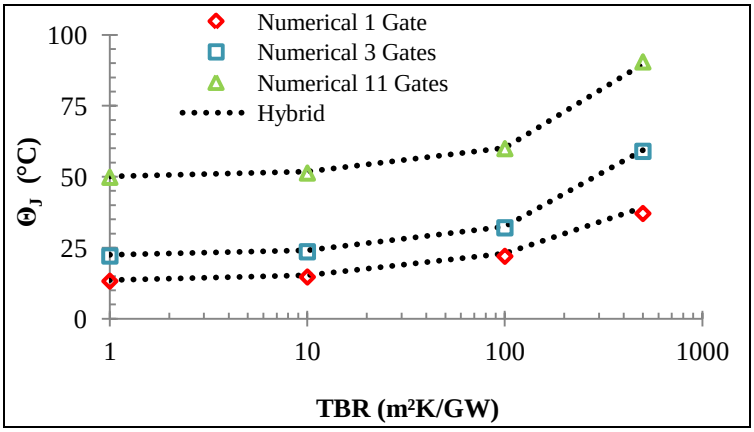


Figure 17. Junction temperature rise as a function of TBR (table 1 parameters).

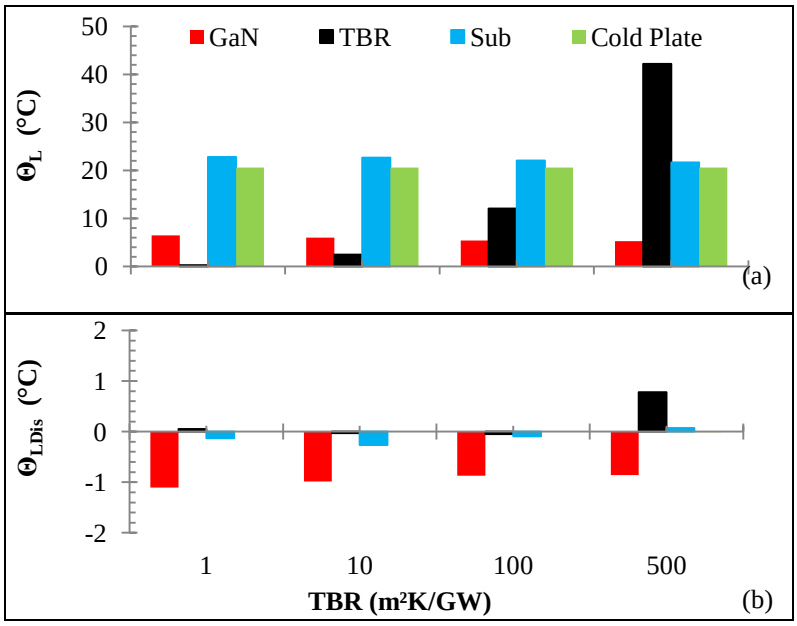


Figure 18. (a) Hybrid model layer temperature rise as a function of TBR and (b) layer temperature rise discrepancy (table 1 parameters).

There exists little discrepancy as a function of TBR as apparent by viewing the layer discrepancies in figure 18b. The source of the small GaN layer discrepancy arises from the previously mentioned uniform heat flux simplification, which causes an artificial increase in spreading resistance when compared to the numerical model. Also, the small discrepancy at high TBR comes from the previously mentioned choice to linearize the GaN thickness impact on spreading width. Overall, these small discrepancies provide confidence with less than 3 °C of discrepancy that the hybrid model is capable of producing accurate junction and layer temperature rise trends for TBR values ranging from 1 to 500 m²K/GW.

5.2 Effect of Gate to Gate pitch

Due to the interaction of multiple heat sources producing increased near junction heat fluxes, the gate to gate pitch has a significant impact on the junction temperature as shown by figure 19. For a fixed gate number, increasing gate to gate pitch decreases the near junction heat flux, allowing the junction temperature to decrease.

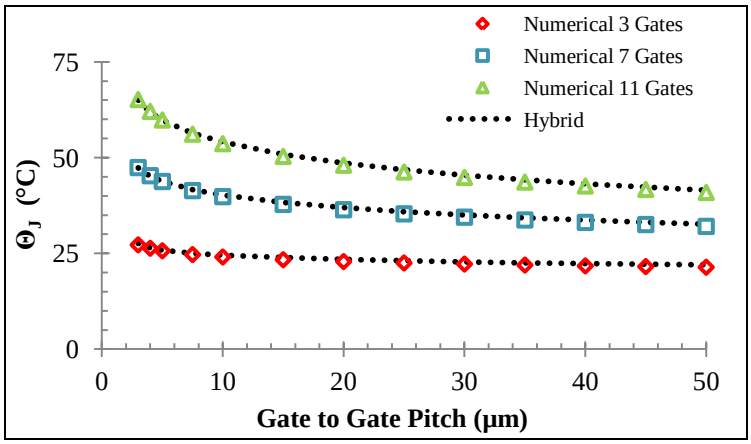


Figure 19. Numerical and hybrid junction temperature rise as a function of pitch and gate number (table 1 parameters).

It is apparent when viewing the hybrid model layer temperature rises in figure 20a that for moderate TBRs the majority of the interaction occurs within the substrate layer, and that little interaction is seen between within the GaN and TBR components for pitches as small as 5 µm. This is expected, as even a pitch of 5 µm is still 5 times larger than the baseline GaN thickness. Thus, the temperature profiles of the GaN and TBR components remain relatively independent of both gate number and pitch, while layers below the interface show direct scaling with gate number and increasing interaction with decreasing pitch.

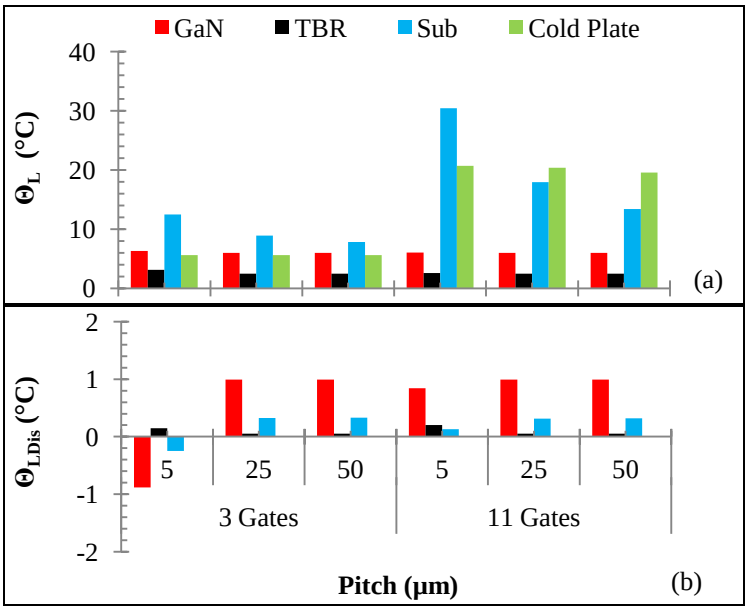


Figure 20. (a) Hybrid model layer temperature rise as a function of pitch and gate number; and (b) layer temperature rise discrepancy as a function of pitch and gate number (table 1 parameters).

Overall, good agreement between the hybrid and numerical models was found, with little difference as shown by figure 20b. The majority of the discrepancy occurs in the GaN layer temperature rise. This suggests the likely source of error to be the simplified heat flux boundary condition. Nonetheless, the total junction discrepancies are less than 5 °C, and individual component discrepancy is about 1 °C or less, providing confidence that the hybrid model can deliver acceptable estimates of junction and layer temperature rise for 3 to 50 μm gate-to-gate pitches.

5.3 Effect of Substrate Thickness

Thinning of the substrate can provide thermal benefits as shown by figure 21. The behavior shown is due to the tradeoff between the substrate and cold plate temperature rise and is clear viewing the hybrid model component temperature rises in figure 22a.

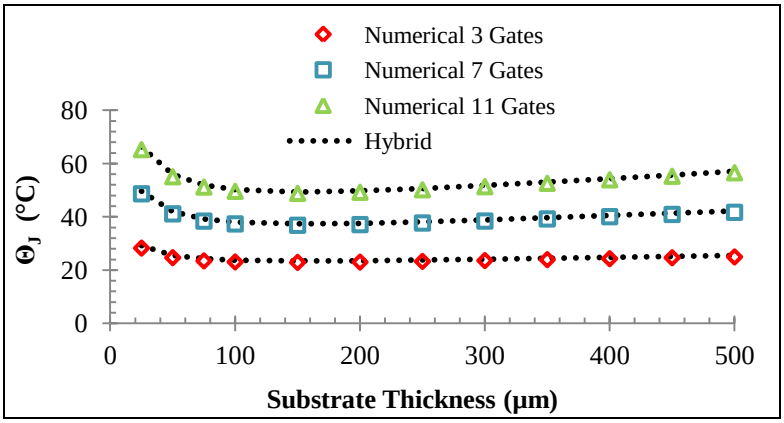


Figure 21. Numerical and hybrid junction temperature rise as a function of substrate thickness and gate number (table 1 parameters).

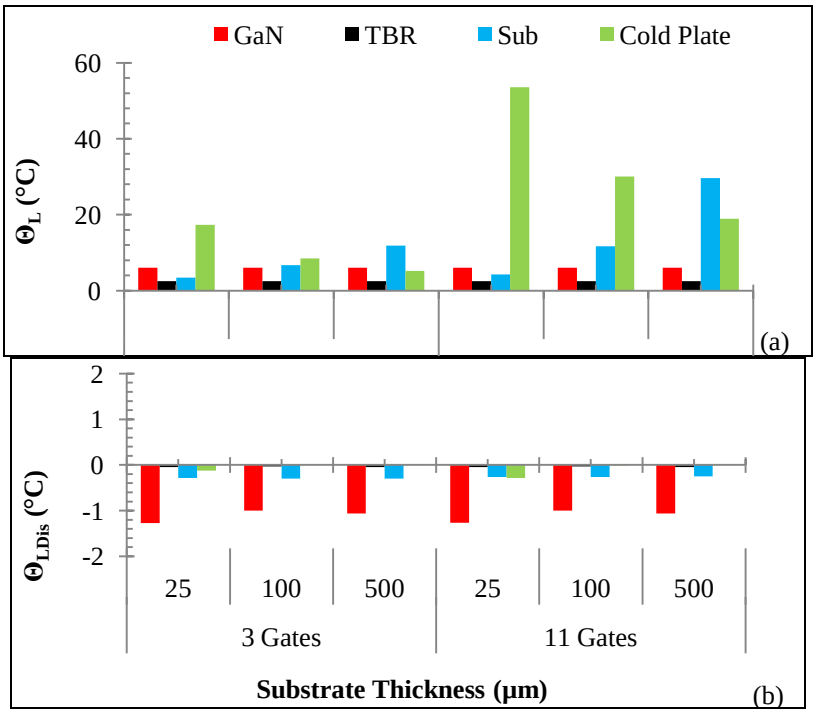


Figure 22. (a) Hybrid model layer temperature rise; and (b) layer temperature rise discrepancy (table 1 parameters).

For thick substrates where the heat is mostly spread before it has entered the cold plate, the low cold plate temperature rise is offset by a large substrate temperature rise because of 1-D conduction. These opposing effects are balanced at around 150 µm independently of TBR or gate number for the geometries studied. The hybrid model accurately demonstrates trends as a function of substrate thickness as shown by figure 22b. Again, the source of the small but constant GaN layer discrepancy lies in the simplified uniform heat flux applied to the top of the GaN. The small total junction temperature discrepancy (<–3 °C) provides confidence that the hybrid model can produce junction and layer temperature rise trends within the 25–500 µm substrate thickness range.

5.4 Effect of GaN Thickness

The GaN thickness is typically chosen for electrical and material quality reasons, but its thickness uniquely influences the junction temperature behavior. On the low end of GaN-on-SiC TBR values (10 m²K/GW), the junction temperature remains relatively independent of GaN thickness as illustrated by figure 23. This trend, however, differs at other TBR values as previously discussed in reference 14 and shown in figure 24.

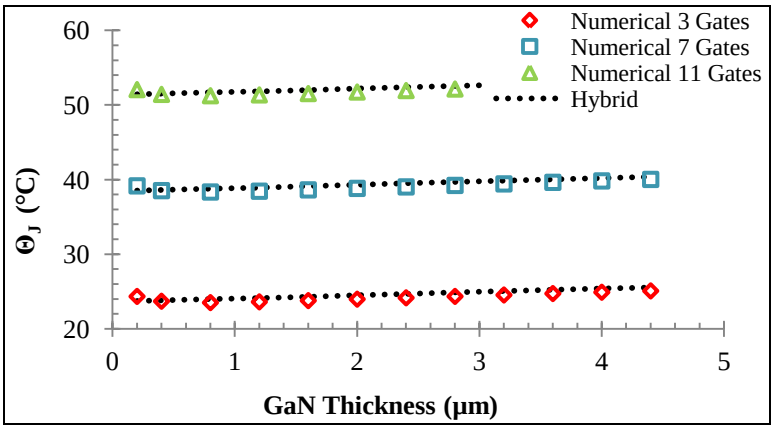


Figure 23. Numerical and hybrid junction temperature as function of GaN thickness and gate number (table 1 parameters).

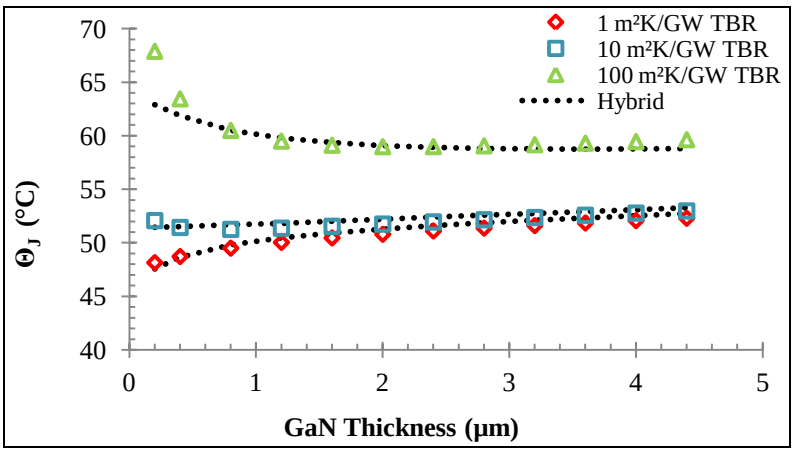


Figure 24. Numerical and hybrid junction temperature as function of GaN thickness and TBR (table 1 parameters).

Differing from the single-gate devices modeled in reference 14, the decrease of GaN thickness provides only a minimal improvement in total junction temperature at small TBRs. This occurs mainly because of the relative dominance of the substrate and cold plate for larger gate numbers, as discussed previously. For larger TBRs, the junction temperature increases as the GaN thickness decreases suggesting the GaN spreading; the TBR tradeoff is shown in figure 25. A device with a large GaN thickness spreads heat within its GaN layer before crossing the TBR, causing a large GaN temperature rise and small TBR temperature rise. However, at small GaN thicknesses, the heat does not spread as much within the GaN and crosses the TBR with a high local heat flux. This produces a substantial TBR temperature rise and a smaller GaN temperature rise. In between these two extremes exists a GaN thickness, which provides a minimum temperature, which is in line with the results from reference 14.

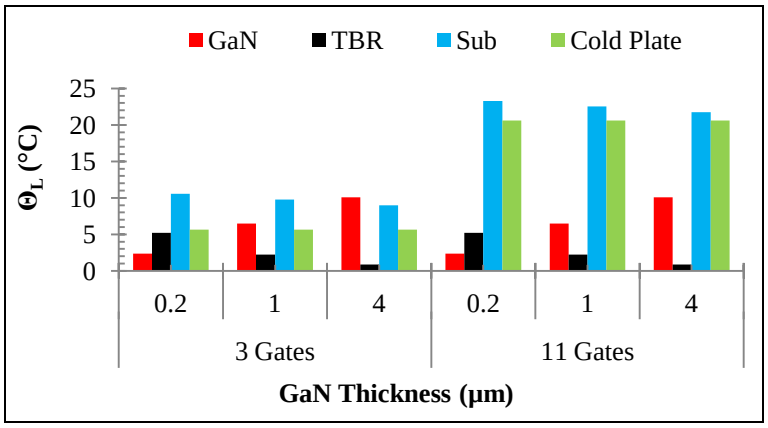


Figure 25. Hybrid model layer temperature rise as function of GaN thickness and gate number (table 1 parameters).

The hybrid model accurately replicates trends for all GaN thickness studied at moderate TBRs. As shown by figure 23, the hybrid model follows the numerical trends with only small differences. From 1 to 100 m²K/GW TBR, the junction total temperature discrepancy only reaches 5 °C, as shown in figure 26a. This discrepancy increases dramatically at the extreme 500 m²K/GW TBR due to the spreading width linearization, as shown in figure 26b. Fortunately references 11, 12 and 32 have demonstrated GaN/SiC TBR values to exist between 10 and 70 m²K/GW. If the need to model the extreme 500 m²K/GW TBR at GaN thicknesses less than 1 µm arises, the spreading width equation (equation 6) can be modified to capture the true nonlinear GaN thickness impact.

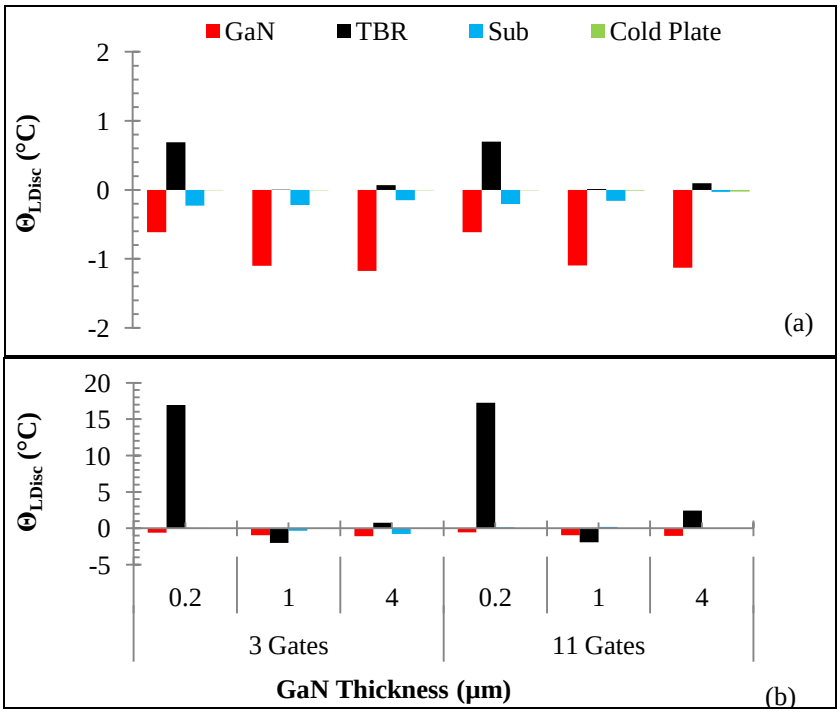


Figure 26. (a) Layer temperature rise discrepancy as a function of GaN thickness and gate number for 10 m²K/GW and (b) Layer temperature rise discrepancy for 500 m²K/GW TBR (table 1 parameters).

5.5 Effect of Substrate Thermal Conductivity

Increasing the substrate thermal conductivity significantly reduces the junction temperature rise, as shown by figure 27. For all cases studied, the temperature reduction observed by the equivalent of replacing Si (100–150 W/mK) with SiC (~400 W/mK) is more dramatic than replacing SiC with near crystal quality diamond (~2000 W/mK). This asymptotic behavior is explained in figure 28, where the substrate spreading and linear thermal resistances reduce quickly making the other components dominate.

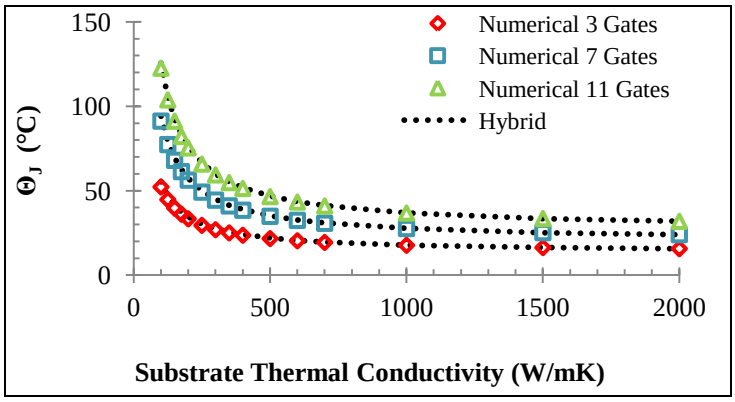


Figure 27. Numerical and hybrid junction temperature rise as a function of substrate thermal conductivity and gate number (table 1 parameters).

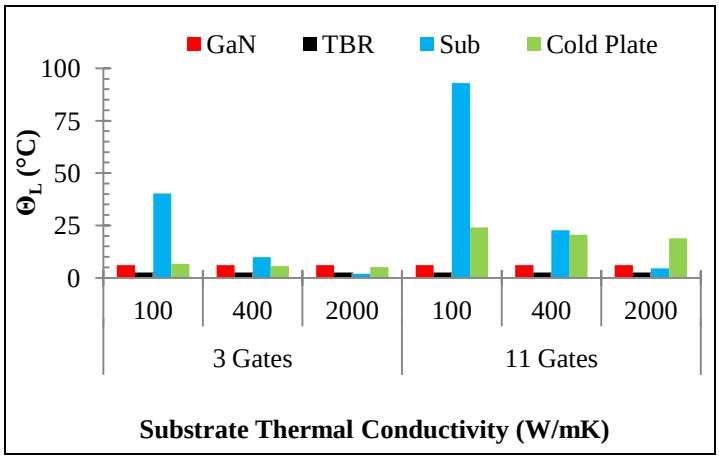


Figure 28. Hybrid model layer temperature rise as function of substrate thermal conductivity (table 1 parameters).

The interaction between substrate conductivity and TBR is shown in figure 29, where increasing the TBR beyond the 10–70 m²K/GW GaN-on-SiC range dramatically shifts the junction temperature rise trend upwards. In the light of this data, it is also worth noting that GaN devices that have been transferred to diamond substrates use an attachment processes with undetermined impact on TBR relative to what it was on the growth substrate (*26*). Thus, over the range of parameters investigated here, the replacement of the SiC with the higher thermal conductivity diamond (~400 vs. ~2000 W/m²K) appears to only be advantageous if the TBR does not increase substantially beyond the 10–70 m²K/GW GaN on SiC range (*11*, *14*).

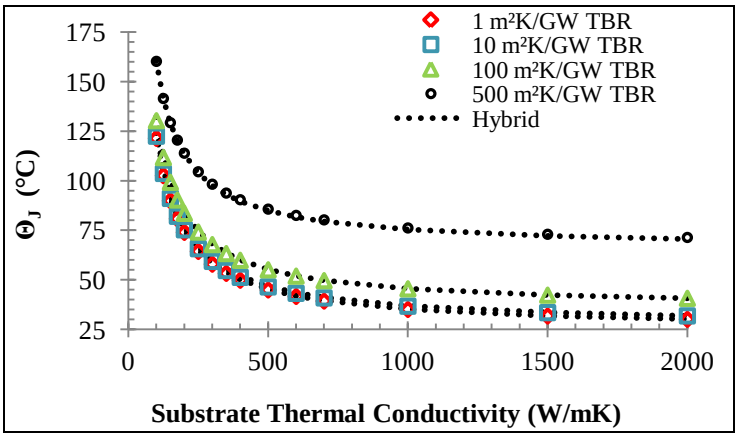


Figure 29. Numerical and hybrid junction temperature rise as a function of substrate thermal conductivity TBR (table 1 parameters).

The hybrid model accurately demonstrates trends as a function of substrate thermal conductivity. As shown by figures 27 and 29, the hybrid model follows the numerical trend with negligible difference. The main source of this discrepancy, shown in figure 30, is the substrate layer component. The small substrate layer discrepancy is visible at low (~100 W/mK) thermal conductivities due to the simplification of the lower layer input heat flux from a “bell-like” to a

top-hat profile. Even so, the total discrepancies are small enough (<5 °C) as to conclude the hybrid model can capture junction and layer temperature rise trends within the 100–2000 W/mK substrate thermal conductivity range of primary interest.

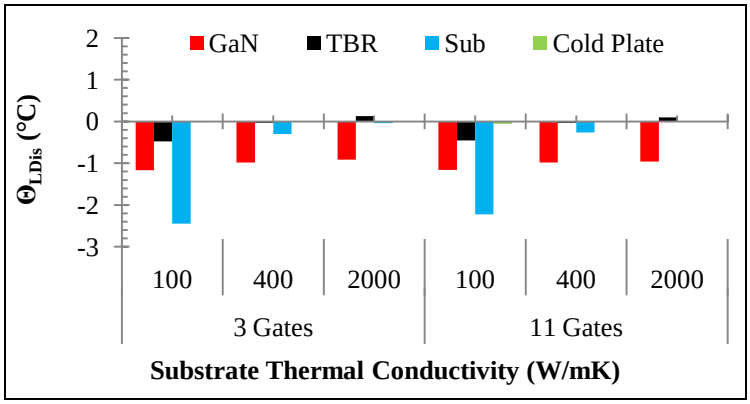


Figure 30. Layer temperature rise discrepancy as a function of substrate thermal conductivity and gate number (table 1 parameters).

6. Conclusion

The push toward higher power and higher power density RF devices has created a number of thermal challenges relating to heat removal and thermal performance prediction. In addition, while there are a large number of parameters available to device designers attempting to improve performance, there is a lack of computationally efficient design models capable of accurately predicting the impact of important parameter changes. The hybrid model presented here combines numerically determined interior spreading widths with an analytical spreading model. An approximate formula for the numerical spreading widths is provided, permitting future designers to avoid full numerical simulations within the parametric bounds stated in table 2. Comparing the hybrid model to its numerical counterpart for the device parameters demonstrates the existence of little discrepancy, except when very large TBRs (~500 m²K/GW) are coupled with GaN thicknesses below 1.5 µm. In most other cases, total junction temperature discrepancy is typically below 5 °C, with an individual temperature component discrepancy of about 1 °C or less.

GaN HEMT devices were modeled using both the new hybrid method and full numerical simulations, varying several structural and thermal parameters to better understand the impact on device thermal performance. This evaluation expanded upon our previous numerical simulations by incorporating the effects of multiple gates. This modeling showed that where TBR was a dominant effect for single-gate devices, GaN and TBR thermal contributions to total junction temperature rise stay relatively constant with gate number and pitches down to 5 µm. Alternatively, the thermal profiles in the substrate layers and below show strong interaction

between gates, and the magnitude of those components scale directly with the number of gates and increase significantly as the gates get closer together. The general trends in component behavior still agree with the single gate models, including the existence of finite substrate and GaN thicknesses producing minimum temperature rise dependent on downstream resistance. Also agreeing with the single gate models, the replacement of the SiC substrate with the higher thermal conductivity diamond appears to only be advantageous if the TBR does not increase substantially beyond the SiC range.

7. References

1. Kemerley, R. T.; Wallace, H. B.; Yoder, M. N. Impact Wide Bandgap Microwave Devices on DoD Systems, in *Proceedings of the IEEE* **2002**, *90* (6), 1022–1031.
2. Mishra, U. K.; Parikh, P.; Wu, Y.-F. AlgaN/GaN HEMTs-An Overview of Device Operation and Applications, *Proceedings of the IEEE* **2002**, *90* (6), 1059–1064.
3. Shealy, J. R.; Kaper, V.; Tilak, V.; Prunty, T.; Smart, J. A.; Green, B.; Eastman, L. F. An AlxGaN1-x/GaN high-electron-mobility transistor with an AlN sub-buffer layer. *Journal of Physics Condensed Matter* **2002**, *14* (13), 3499–3509.
4. Felbinger, J. G.; Chandra, M.V.S.; Yunju Sun, Eastman, L. F.; Wasserbauer, J.; Faili, F.; Babic, D.; Francis, D.; Ejeckam, F. Comparison of GaN HEMTs on Diamond and SiC Substrates. *IEEE Electron Device Letters* **2007**, *28* (11), 948–950.
5. Smith, A. N.; Calame, J. P. Impact of Thin Film Thermophysical Properties on Thermal Management of Wide Bandgap Solid-State Transistors. *International Journal of Thermophysics* **2004**, *25* (2), 409–422.
6. Calame, J. P.; Myers, R. E.; Wood, F. N.; Binari, S. C. Simulations of Direct-Die-Attached Microchannel Coolers for the Thermal Management of GaN-on-SiC Microwave Amplifiers. *IEEE Transactions on Components and Packaging Technologies* **2005**, *28* (4), 797–809.
7. Calame, J. P.; Myers, R. E.; Binari, S. C.; Wood, F. N.; Garven, M. Experimental investigation of microchannel coolers for the high heat flux thermal management of GaN-on-SiC semiconductor devices. *International Journal of Heat and Mass Transfer* **2007**, *50* , 4767–4779.
8. Darwish, A. M.; Bayba, A. J.; Hung, H. H. Thermal Resistance Calculation of AlxGaN1-x-GaN Devices. *IEEE Transaction on Microwave Theory and Techniques* **2004**, *52* (11), 2611–2620.
9. Darwish, A. M.; Bayba, A. J.; Hung, H. H. Accurate Determination of Thermal Resistance of FETs. *IEEE Transaction on Microwave Theory and Techniques* **2005**, *53* (1), 306–313.
10. Douglas, E. A.; Ren, F.; Pearton, S. J. Finite-element simulations of the effect of device design on channel temperature for AlxGaN1-x/GaN high electron mobility transistors, Journal of Vacuum Science & Technology B: *Microelectronics and Nanometer Structures* **2011**, *29* (2), 020603–020603-4.

11. Manoi, A.; Pomeroy, J. W.; Killat, N.; Kuball, M.; 2010, Benchmarking of Thermal Boundary Resistance in AlxGaN1-x/GaN HEMTs on SiC Substrates: Implications of the Nucleation Layer Microstructure. *IEEE Electron Device Letters* **2010**, *31* (12), 1395–1397.

12. Riedel, G. J.; Pomeroy, J. W.; Hilton, K. P.; Maclean, J. O.; Wallis, D. J.; Uren, M. J.; Martin, T.; Forsberg, U.; Lundskog, A.; Kakanakova-Georgieva, A.; Pozina, G.; Janzen, E.; Lossy, R.; Pazirandeh, R.; Brunner, F.; Wurfl, J.; Kuball, M. Reducing Thermal Resistance of AlxGaN1-x/GaN Electronic Devices Using Novel Nucleation layers. *IEEE Electron Device Letters* **2009**, *30* (2), 103–106.

13. Cho, J. ; Bozorg-Grayeli, E.; Altman, D. H.; Asheghi, M.; Goodson, K. E. Low thermal resistances at GaN-SiC interfaces for HEMT technology. *IEEE Electron Device Lett.* **2012**, *33*, 378–380.

14. Nochetto, H.; Jankowski, N.; Bar-Cohen, A. ; The Impact of GaN/Substrate thermal boundary resistance on a HEMT device, in *Proceedings of the ASME 2011 International Mechanical Engineering Congress & Exposition*, Denver, CO, **2011**,*10*, 241–249

15. Yovanovich, M.; Muzychka, Y.; Culham, J. Spreading Resistance of Isoflux Rectangles and Strips on Compound Flux Channels. *Journal of Thermophysics and Heat Transfer* **1999**, *13* (4), 495–500.

16. Muzychka, Y.; Culham, J.; Yovanovich, M. Thermal Spreading Resistance of Eccentric Heat Sources on Rectangular Flux Channels. *Journal of Electronic Packaging* **2003**, *125* (4), 179–185.

17. Meneghesso, G.; Verzellesi, G.; Danesin, F.; Rampazzo, F.; Zanon, F.; Tazzoli, A.; Meneghini, M.; Zanoni, E. Reliablity of GaN High-Electron-mobility Transistors: State of the Art and Perspectives. *IEEE Transaction on Device and Materials Reliability* **2008**, *8* (2), 332–343.

18. Sarua, A.; Ji, H.; Kuball, M.; Uren, M. J.; Martin, T.; Hilton, K. P.; Balmer, R. S. Integrated Micro-Raman/Infrared Thermography Probe for Monitoring of Self-Heating in AlxGaN1-x/GaN Transistor Structures. *IEEE Transactions on Electron Devices* **2006**, *53* (10), 2438–2447.

19. Liu, W.; Baladin, A. Thermal conduction in $Al_xGa_{1-x}N$ alloys and thin films. *Journal of Applied Physics* **2006**, *97* (073710), 1–6.

20. Bar-Cohen, A.; Albrecht, J.; Maurer, J. Near Junction Thermal Management for Wide Bandgap Devices. *Compound Semiconductor Integrated Circuit Symposium*, 1–5, 2011.

21. Kuball, M.; Rajasingam, S.; Sarua, A.; Uren, M. J.; Martin T.; Jughes, B. T. et al. Measurement of temperature distribution in multifinger AlxGaN1-x/GaN heterostructure field-effect transistors using micro-Raman spectroscopy. *Applied Physics Letters* **2003**, *82* (1), 124–126.

22. Heller, E. R.; Crespo, A. Electro-thermal modeling of multifinger AlxGaN1-x/GaN HEMT device operation including thermal substrate effects. *Microelectronics Reliability* **2008**, *48* (1), 45–50.

23. Yamanaka, M.; Mori, K.; Iyomasa, K.; Phtsuka K.; Noto, H.; Nakayama, M.; Kamo, Y.; Isota, Y. C-band GaN HEMT Power Amplifier with 220W output Power. in *Proceedings of IEEE Microwave Symposium*, IEEE, Honolulu, HI, 1251–1254, 2007.

24. Kamo, Y.; Kunii, T.; Takeuchi, H.; Yamamoto, Y.; Totsuka, M.; Shiga, T.; Minami, H.; Kitano, T.; Miyakuni, S.; Oku, T.; Inoue, A.; Matsuda, Y.; Ishikawa, T.; Nanjo, T.; Chiba, H.; Suita, M.; Oishi, T.; Abe, Y.; Tsuyama, Y.; Shirahana, R., Ohtsuka, H.; Iyomasa , K., Yamanaka, K.; Hieda, M.; Nakayama, M.; Takagi, T.; Marumoto, K.; A C-Band AlxGaN1-x/GaN HEMT with Cat-CVD SiN passivation developed for an over 100W operation. in *Proceedings of Microwave Symposium Digest*, 495–498, 2005.

25. Jessen, G. H.; Gillespie, J. K.; Via, G. D.; Crespo, A.; Langley, D.; Felbinger, J.; Wasserbauer, J.; Faili, F.; Babic, D.; Ejeckam, F.; Guo, S.; Eliashevich, I. AlxGaN1-x/GaN HEMT on Diamond Technology Demonstration. in *Proceedings of the Compound Semiconductor Integrated Circuit Symposium*, IEEE, San Antonio, TX, 271–274, 2006.

26. Chabak, K. D.; Gillespie, J. K.; Miller, V.; Crespo, A.; Roussos, J.; Trejo, M.; Walker, D. E.; Via, G. D.; Jessen, G. H.; Wasserbauer, J.; Faili, F.; Babic, D. I.; Francis, D.; Ejeckam, F. Full-Wafer Characterization of AlxGaN1-x/GaN HEMTs on Free-Standing CVD Diamond Substrates. *IEEE Electron Device Letters* **2010**, *31* (2), 99–101.

27. Brown, J.; Borges, R.; Piner, E.; Vescan, A.; Singhal, S.; Therrien, R. AlxGaN1-x/GaN HFETs fabricated on 100mm GaN on silicon (111) substrates. *Solid-State Electronics* **2000**, *46* (10), 1535–1539

28. Radhakrishnan, K.; Dharmarasu, N.; Sun, Z.; Arulkumaran, S.; Ng, G. I. Demonstration of AlxGaN1-x/GaN high-electron-mobility transistors on 100mm diameter Si(111) by plasma-assisted molecular beam epitaxy. *Applied Physics Letters* **2010**, *97*, 232107–1-3.

29. Taking, S.; Banerjee, A.; Zhou, H.; Li, X.; Khokhar, A. Z.; Oxland, R.; McGregor, I.; Bentley, S.; Rahman, F.; Thayne, I.; Dabiran, A.M.; Wowchak, A. M.; Cui, B.; Wasige, E. Surface passivation of AIN/GaN MOS-HEMTs using ultra-thin Al_20_3 formed by thermal oxidation of evaporated aluminum. *Electronics Letters* **2010**, *46* (4), 301–302.

30. Selvaraj, S. L.; Suzue, T.; Egawa, T. Breakdown Enhancement of AlxGaN1-x/GaN HEMTs on 4-in Silicon by Improving the GaN Quality on Thick Buffer Layers. *IEEE Electron Device Letters* **2009**, *30*(6), 587–589.

31. Filippov, K. A.; Balandin, A. A. The effect of the thermal boundary resistance on self-heating of AlxGaN1-x/GaN HFETs. *MRS Internet Journal of Nitride Semiconductor Research* **2003**, *8* (4), 1-3.

32. Sommet, R.; Mouginot, G.; Quére, R.; Ourach, Z.; Heckmann, S.; Camiade, M. Thermal Modeling and Measurements of AlxGaN1-x/GaN HEMTs including thermal Boundary Resistance. in *Proceedings of the 16th International Workshop on Thermal Investigations of ICs and Systems*, Barcelona, Spain, 271-274, 2010.

33. Zhao, Y.; Zhu, C.; Wang, S.; Tian, J. Z.; Yang, D. J.; Chen, C. K.; Cheng, H.; Hing, P. Pulsed photothermal reflectance measurement of the thermal conductivity of sputtered aluminum nitride thin films. *Journal of Applied Physics* **2004**, *96* (8), 4563–4568.

34. Zou, J.; Kotchetkov, D.; Balandin, A. A.; Florescu, D. I.; Pollak, F. H. Thermal conductivity of Gan films: Effects of impurities and dislocations. *Journal of Applied Physics* **2002**, *92* (5), 2534–2539.

35. Garven, M.; Calame, J. Simulation and Optimization of Gate Temperature sin GaN-on-SiC Monolithic Microwave Integrated Circuits. *IEEE Transaction on Components and Packaging Technologies* **2009**, *31* (1), 63–72.

36. Mishra, U. K.; Shen, L.; Kazior, T. E.; Wu, Y.F. GaN-Based RF Power Devices and Amplifiers. *Proceedings of the IEEE* **2008**, *96* (2), 287–305.

37. Wu, Y.-F.; Moore, M.; Saxler, T.; Wisleder, T.; Parikh, P. 40-W/mm double field-plated GaN HEMTs. in *Proceedings of the IEEE 64th Device Research Conference*, IEEE, State College, PA,151–152, 2006.

38. Nochetto, H. Hotspot Remediation Using Germanium Self Cooling Technology, Thesis, University of Maryland, College Park, MD, 2011.

List of Symbols, Abbreviations, and Acronyms

2-D	two dimensional
3-D	three dimensional
AIN	aluminum nitride
Al_xGaN_{1-x}	aluminum gallium nitride
DoD	Department of Defense
DMM	diffuse mismatch model
FEA	finite element analysis
GaN	gallium nitride
h_{CP}	effective heat transfer coefficient (W/m^2K)
HEMT	high electron mobility transistor
h_{GaN}	coupling heat transfer coefficient (W/m^2K)
L*	spreading width (μm)
MMIC	monolithic microwave integrated circuit
MOCVD	metal-organic chemical vapor deposition
PA	power amplifier
$q_{s'}$	single heat source (W/mm)
R_{CP}	total thermal resistance due to cold plate (°C/W)
RF	radio frequency
R_{GaN}	total thermal resistance due to GaN (°C/W)
R_{Sub}	total thermal resistance due to substrate (°C/W)
R_{TBR}	thermal resistance due to TBR (°C/W)
Si	silicon
SiC	silicon carbide
TBR	thermal boundary resistance (m^2K/GW)

T_C	coolant temperature (°C)
$T_{CP(x)}$	cold plate temperature distribution (°C)
$T_{GaN(x,y)}$	temperature distribution within GaN (°C)
$T_{MG(x)}$	multiple gate temperature distribution (°C)
$T_{S(x)}$	single gate temperature distribution (°C)
T_{SGJ}	single gate junction temperature (°C)
$T_{Sub(x,y)}$	temperature distribution within substrate (°C)
$T_{TB(x)}$	TBR temperature distribution (°C)
$\Delta T_{Num,TBR}$	numerically determined TBR temperature rise (°C)
Θ_C	cold plate to case temperature rise (°C)
Θ_{GaN}	GaN temperature rise (°C)
Θ_{Hybrid}	hybrid model component temperature rise (°C)
Θ_J	junction to case temperature rise (°C)
$\Theta_{L,Dis}$	component discrepancy (°C)
Θ_{Num}	numerical component temperature rise (°C)
Θ_{Sub}	substrate temperature rise (°C)
Θ_{TBR}	TBR temperature rise (°C)

1 (PDF only) DEFENSE TECHNICAL INFORMATION CTR
DTIC OCA
8725 JOHN J KINGMAN RD
STE 0944
FORT BELVOIR VA 22060-6218

1 DIRECTOR
US ARMY RESEARCH LAB
IMAL HRA
2800 POWDER MILL RD
ADELPHI MD 20783-1197

1 DIRECTOR
US ARMY RESEARCH LAB
RDRL CIO LL
2800 POWDER MILL RD
ADELPHI MD 20783-1197

1 DIRECTOR
US ARMY RESEARCH LAB
RDRL CIO LT
2800 POWDER MILL RD
ADELPHI MD 20783-1197

6 US ARMY RSRCH LAB
ATTN RDRL SED E SHAFFER
ATTN RDRL SED E L BOTELER
ATTN RDRL SED E P BARNES
ATTN RDRL SED E A LELIS
ATTN RDRL SED E K JONES
ATTN RDRL SER E A HUNG
2800 POWDER MILL RD
ADELPHI MD 20783-1197

1 DARPA
MICROSYSTEMS TECHNOLOGY OFFICE PROGRAM MANAGER
AVRAM BAR-COHEN
DARPA-MTO, RM 06-156
675 NORTH RANDOLPH STREET
ARLINGTON, VA 22203-2114

INTENTIONALLY LEFT BLANK.